AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A semiconductor integrated circuit comprising:

a boundary scan test circuit for testing, after said semiconductor integrated circuit is mounted on a printed circuit board, ~~the~~ a mounted state of said semiconductor integrated circuit;

a first pad having a potential level set according to a type of a package in which said semiconductor integrated circuit is sealed; and

control circuitry for fixedly setting said boundary scan test circuit to either one of an operable state and an operation disabled state according to the potential level of said first pad.

2. (Original) The semiconductor integrated circuit according to claim 1, wherein

said boundary scan test circuit comprises a buffer circuit coupled to a second pad to generate an internal signal according to an externally applied signal via said second pad in an operable state, and

said control circuitry comprises a circuit for selectively setting said buffer circuit to the operable state or to the operation disabled state in accordance with the potential level at said first pad.

3. (Original) The semiconductor integrated circuit according to claim 1, wherein said type of the package includes a surface mount type flat package and a solder ball array arrangement type package.

4. (Original) The semiconductor integrated circuit according to claim 3, wherein said control circuitry includes a circuit for setting said boundary scan test circuit to the operable state

when the type of the package is the solder ball array arrangement type package and to the operation disabled state when the type of the package is the surface mount type flat package.

5. (Original) The semiconductor integrated circuit according to claim 2, wherein the type of the package includes a surface mount type flat package and a solder ball array arrangement type package, and said control circuitry includes a circuit for setting said buffer circuit into the operable state when the type of the package is the solder ball array arrangement type package and to the operation disabled state to fix an output signal of said buffer circuit to a predetermined logical level when the package is the surface mount type flat package.

6. (Original) The semiconductor integrated circuit according to claim 1, wherein

said boundary scan test circuit comprises a first logic gate having a first input coupled to a second pad and a second input,

said control circuitry comprises

a first set circuit for generating a signal of a potential according to a potential of said first pad, and

a second logic gate applying a signal to the second input of said first logic gate that sets said first logic gate to one of the operable state and the operation disabled state, according to an output signal of said first set circuit.

7. (Original) The semiconductor integrated circuit according to claim 6, wherein said first set circuit includes means for generating a function setting signal for setting a function implemented by said semiconductor integrated circuit in accordance with the potential at said first pad.

8. (Original) The semiconductor integrated circuit according to claim 6, wherein said first set circuit includes means for generating an operation mode designation signal placing the semiconductor integrated circuit in an operation mode designated by said operation mode designated signal.

9. (Original) The semiconductor integrated circuit according to claim 1, wherein

said boundary scan test circuit comprises a first logic having a first input coupled to a second pad and a second input,

said control circuitry comprises

a first set circuit for generating a signal of a potential according to a potential of said first pad,

a second set circuit for generating a signal of a potential according to a potential of a third pad, and

a second logic gate receiving an output signal of said first set circuit and an output signal of said second set circuit to perform a logic process thereon, and applying a resultant signal to the second input of said first logic gate.

10. (Original) The semiconductor integrated circuit according to claim 6, wherein said function set circuit comprises

a first transistor for setting said first pad to a first logic level in response to starting of application of power supply voltage,

an inverter circuit inverting a logic level of the potential of said first pad to output a signal corresponding to an output signal of said first set circuit, and

a second transistor connected in parallel to said first transistor, between said first pad and a power source node applying a potential of said first logic level, and receiving an output signal of said inverter circuit at a control electrode node thereof.

11. (Original) The semiconductor integrated circuit according to claim 9, wherein said second set circuit comprises

a first transistor for setting said third pad to the potential level of a first logic level in response to starting of application of a power supply voltage,

an inverter circuit inverting a logic level of a potential of said third pad to output a signal corresponding to an output signal of said second set circuit, and

a second transistor connected in parallel to said first transistor, between said third pad and a power source node applying a potential at said first logic level, and receiving an output signal of said inverter circuit at a control electrode node thereof.

12. (Currently Amended) A semiconductor integrated circuit comprising:

a pad;

a first transistor for setting said pad to a voltage level of a first logic level in response to application of a power supply voltage to power up said semiconductor integrated circuit;

an inverter for inverting a logic of a potential on said pad; and

a second transistor connected in parallel to said first transistor, and receiving an output signal of said inverter at a control electrode node thereof;

an operation mode of an internal circuit being specified by an output signal of said inverter.

13. (Original) The semiconductor integrated circuit according to claim 12, further comprising a transfer gate inserted between said pad and an input of said inverter, receiving a fixed potential at a control electrode node thereof.

14. (Currently Amended) The semiconductor integrated circuit according to claim 12, further comprising a protection circuit coupled to said pad for absorbing an excess voltage higher in absolute value than a first power supply voltage generated at said ~~paid~~ pad, and wherein

said inverter operates using a second power supply voltage lower in absolute value than said first power supply voltage as an operating power supply voltage.

15. (Currently Amended) The semiconductor integrated circuit according to claim 14, further comprising a transfer gate connected between said protection circuit and an input of said ~~protector~~ inverter and receiving said second power supply voltage at a control gate thereof.

16. (Original) The semiconductor integrated circuit according to claim 15 wherein the first and second transistor are connected in parallel between the input of said inverter and a node supplying said second power supply voltage.

17. (Original) The semiconductor integrated circuit according to claim 12, wherein said inverter operates using a first power supply voltage as one operating power supply voltage, and said semiconductor integrated circuit further comprises a level converter for converting an amplitude of the output signal of said inverter to an amplitude of a second power supply voltage higher than the first power supply voltage.

18. (Original) The semiconductor integrated circuit according to claim 12, wherein said paid comprises a bonding option pad.